

IN THE CLAIMS:

Claim 1 (Cancelled).

2. (Currently Amended) The method for fabricating a semiconductor device of Claim [1] 7, further comprising a step of forming, on said buried interconnect, a third insulating film for preventing diffusion of a metal included in said buried interconnect.

3. (Currently Amended) The method for fabricating a semiconductor device of Claim [1] 7,

wherein both of said first insulating film and said second insulating film include inorganic materials as principal constituents, and

the step of forming said first interconnect groove includes a sub-step of forming a second interconnect groove in a second region, which is different from the first region, of said [planarized] second insulating film through selective etching using said second mask pattern.

4. (Currently Amended) The method for fabricating a semiconductor device of Claim [1] 7,

wherein said first insulating film includes an organic material as a principal constituent and said second insulating film includes an inorganic material as a principal constituent, and

the step of forming said first interconnect groove includes a sub-step of forming a second interconnect groove in a second region, which is different from the first region, of said [planarized] second insulating film through selective etching using said second mask pattern in forming an upper portion of said first interconnect groove in said thinned portion of said second insulating film through the selective etching using said second mask pattern.

5. (Currently Amended) The method for fabricating a semiconductor device of Claim 4,

wherein the step of forming said first interconnect groove includes a sub-step of removing said second mask pattern in forming a lower portion of said first interconnect groove in said first insulating film [through the selective etching using said second mask pattern].

6. (Currently Amended) The method for fabricating a semiconductor device of Claim [1] 7,

wherein said thinned portion of said second insulating film has a thickness of 10 nm through 50 nm.

7. (New) A method for fabricating a semiconductor device comprising the steps of:
forming, on a substrate, a first insulating film with a relatively low dielectric constant and low mechanical strength;

A partially retaining said first insulating film in a first region through selective etching using a first mask pattern formed on said first insulating film;

forming a second insulating film with a relatively high dielectric constant and high mechanical strength, such that said second insulating film covers said retained first insulating film;

forming a thinned portion of said second insulating film on said retained first insulating film by planarizing said second insulating film by polishing;

forming a first interconnect groove in said thinned portion of said second insulating film and said retained first insulating film through selective etching said thinned portion of said second insulating film and said retained first insulating film using a second mask pattern formed on said thinned portion of said second insulating film; and

forming a buried interconnect in said first interconnect groove,
whereby said thinned portion of said second insulating film and said retained first insulating film are provided on the sides of said buried interconnect.

8. (New) The method for fabricating a semiconductor device of Claim 7,
wherein a thickness of said thinned portion of said second insulating film in said first region is smaller than a thickness of said second insulating film in a second region, which is different from said first region.

9. (New) The method for fabricating a semiconductor device of Claim 7,
wherein the step of forming said first interconnect groove includes a sub-step of forming a second interconnect groove in a second region, which is different from said first region, of said second insulating film through selective etching of said second insulating film using said second mask pattern.
